THE CHOICE OF A SIMULATION TIME STEP IN THE REAL-TIME SIMULATOR APPLICATIONS

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Abstract – **This paper discusses one of the most important design and application issues in a real-time digital simulator design, namely the issue of the simulation time-step. A real-time digital simulator for protective relay testing recently developed by Texas A&M University for Western Area Power Administration is used to illustrate various aspects of the simulation time-step issue. Frequency bandwidth, simulation accuracy, network complexity, and I/O subsystem requirements are selected to illustrate how the choice of the simulation time step affects design and application of the simulator.**

Keywords – Digital Simulation, Electromagnetic Transient Program, Real-Time Digital Simulators, Protective Relaying, Relay Testing

I. INTRODUCTION

In the Spring of 1994, Texas A&M University (TAMU) delivered to Western Area Power Administration (WAPA) a digital real-time simulator for relay testing [1-4]. This simulator is built around a commercial, high-performance, single-processor workstation, that hosts a graphical user interface and real-time power system simulation program. An output Digital Signal Processing (DSP) subsystem, that hosts the simulation software for instrument transformers and circuit breakers, is also part of this system. Among other advanced features, this simulator allows a choice of the real-time simulation time step.

One of the most important issues in the design and application of a real-time digital simulator is the size of the simulation time step. It must be carefully considered by both designers and users of the real-time simulators. For the designer, it is important because the choice of the supported time step determines many design criteria that affect the real-time performance of the simulator. For the user it is important because the choice of the simulation time step determines the application characteristics of the simulator.

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This paper deals with the impact of the real-time simulation time step upon TAMU's digital simulator design. The various aspects of the simulation time step are identified in Section II. In Section III, the relations affecting selection of the time step are closely examined. Section IV shows how these relations can be practically used. Various application situations are used to illustrate time-step selection.

II. SIMULATION TIME STEP ASPECTS

A. Frequency Bandwidth

The first aspect of the simulation time step that faces both designers and users of the real-time digital simulator is the frequency bandwidth of its output signals. As the output bandwidth adequately descibes many characteristics of the signals seen by the relay under test, from the relay testing standpoint, bandwidth is more meaningfull than the simulation time step. On the other hand, the simulation time step is the parameter that is dealth with by the users in the every day use of the simulator. Therefore, the relationship between the frequency bandwidth and the simulation time step needs to be clearly understood.

According to Shannon's sampling theorem, the input signal must be sampled with a frequency (f_S), at least twice as high as the cut-off frequency of the signal spectra (f_C), i.e., $f_S \geq 2f_C$, to prevent aliasing. This is the ideal relationship, since in practice various factors make this relationship more conservative. For example, if the required simulator sampling frequency was specified at 20 kHz, a 10 kHz frequency bandwidth would be reproduced according to the sampling theorem. In reality, only frequencies up to about 7 kHz would be reproduced accurately.

The desired frequency bandwidth of the test signals generated by the simulator is determined from an analysis of the input waveform requirements of the relays being tested. For example, for microprocessor-based relay designs working on the principle of estimating the fundamental frequency waveform, the frequency bandwidth requirements start, for a 60 Hz system, from 120 Hz for the relays using 4 samples/cycle and may go as high as 480 Hz for 16 samples/cycle relays. As another example, in the case of the protective relay designs utilizing traveling wave approach, the frequency bandwidth requirements may be much higher.

B. Simulation Accuracy

Closely related to the choice of the simulation time step is the issue of the simulation accuracy. The fact that simulation accuracy depends on the choice of the simulation time step is even intuitively known, but obtaining the actual relationship is quite difficult. In fact, it may be impossible to establish an exact relationship between the overall simulation accuracy and simulation time step. Then, only the accuracy of the simulation of the individual elements of the power system may be analyzed. However, even if such an approach is taken, there are several factors to be considered.

The relationship between the time step and simulation accuracy depends on the choice of the network solution methods. Methods based on the trapezoidal integration rule exhibit a significantly different relationship between the time step and simulation than methods based upon Simpson's integration rule, or first order Runge-Kutta method. The differences between various solution methods become even more exaggerated if higher order, or compensated, integration rules are examined. A thorough understanding of the solution methods used in a particular simulator implementation is necessary if one is to examine the effect of the varying time step upon network elements.

Identifying which one of the network elements has the greatest influence on the overall accuracy of the network simulation is another question. When testing transmission line relays, the transmission line models can be assumed to have the greatest impact on the overall simulation accuracy, but this assumption should be carefully verified. Many other elements, such as line reactors, can have a severe impact on relay performance when not modeled accurately enough.

When testing different types of relays, it may be assumed that different elements will have more of an impact on the simulation accuracy. On the other hand, the relationship between time step and accuracy is much more complex for transmission lines than for simple network elements. Under the circumstances, probably the best method of estimating the accuracy of simulation may be to use the accuracy figures obtained for the individual elements as an indicator of the overall accuracy.

C. Network Complexity

In the real-time transient simulations, one of the main considerations in determining the appropriate simulation time step is the network complexity. For a single processor architecture, such as that used in the TAMU's real-time simulator, the general relation is that the more complex the network to be simulated, the larger the minimum possible simulation time step.

Usually, the network complexity is defined by the number of the nodes in the network (or, roughly, the size of the network matrix). A relation between the number of the nodes and the simulation time step does exist, but it is not the simple one since other factors also contribute to the network complexity. Therefore, it may only be possible to find a general relation between the various measures of the network complexity and the required simulation time step.

As an example, when testing transmission line relays one factor that must be considered is the existence of various transmission line models. Whether the transmission line is represented by distributed parameter line model, or by lumped parameter line model, has a significant impact on the required computation time. Similarly, constant parameter line models and frequency dependent parameter line models yield different levels of network complexity.

A similar reasoning can be applied to modelling nonlinear elements, coupled elements, and switching operations. Also, different solution methods can impact the computational complexity of an element. For example, the presence of the iteratively solved nonlinear models will drastically affect time step. Similarly, the organization of the solution method itself is a very important factor. Methods that use distributed processing tend to have shorter computation times.

D. I/O Subsystem Characteristics

There is certain amount of computational overhead in the output section of the simulator (Fig. 1). Careful analysis of the I/O output subsystem of the TAMU's simulator is necessary to assess that overhead. The first question is the data transfer overhead (1). The organization of the data transfer from the memory of the computer to the output bus of the I/O subsystem may greatly influence the time needed for this operation. Precise measurement and calculation are necessary to access this overhead. Additional overhead in the I/O subsystem may be caused by the instrument transformer simulation (2) if it is done separately using front end simulation subsystem. The size of this overhead depends mostly on the complexity of the instrument transformer models. Next, there is overhead due to conversion between different floating point number representations (3) that may be required. Finally, the communication overhead (4) required to export data from the simulator to the relay under test must be taken into account.

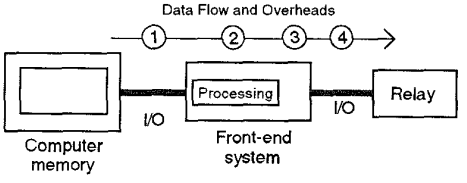

Fig. 1. I/O system overheads

III. TIME STEP SELECTION AND ITS IMPACTS

This section of the paper examines the relations among main factors determining the simulation time step. In particular, TAMU's simulator design is used to demonstrate the impact upon simulator design.

A. Simulator Architecture

The major subsystems of TAMU's real-time digital simulator are shown in Fig. 2.

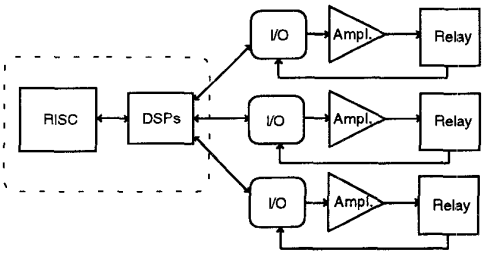

Fig. 2. Real-Time Simulator Architecture

The real-time network transient simulation is performed using custom designed *Real-Time System* (*RTS*) software on a RISC computer. During each time step, a set of samples generated by the simulation is sent to the DSP subsystem where circuit breaker and instrument transformer are simulated. Next, the samples of the test signals are transmitted through the I/O section to the D/A conversion subsystem. There, the analog signals are produced, amplified and submitted to the relay under test. Finally, the trip signals of the relays are collected and returned to the RTS through the I/O and DSP subsystem.

B. Frequency bandwidth

As mentioned earlier, the starting point in defining the frequency bandwidth is the analysis of the requirements of the relay under test. Generally, the bandwidth of 5 to 10 kHz should be adequate for most of the relays. However, one should expect to exploit the capabilities of the simulator to the maximum because of the improvements in the accuracy. Simulator design should be able to support such a practice.

The waveform reconstruction system of the TAMU's simulator supports virtually continuous selection of the sampling rate in the upper range from 3.2 to 35 kS/sec. The upper limit is usually beyond the limit imposed by the complexity of the network model. The I/O system is expected to be a bottleneck only for very simple models that are not frequently used in practice. Even in physically simple power systems, one is usually more interested in increasing the detail of the network model by increasing its complexity, than in achieving an absolute minimum of the time step.

C. Simulation accuracy

Simulation of network transients in TAMU's real-time digital simulator is performed by the *Real-Time System* (*RTS*) software. It is an electromagnetic transients simulation program especially written for the real-time applications.

The *RTS* uses the same solution method as industry standard *Electromagnetic Transient Program* (*EMTP*) [5]. To obtain transient solution for the network, *RTS* solves the matrix equation: $[G]\cdot[v(t)]=[h(t)]$, where [G] is the matrix of the node conductances, [v(t)] is the vector of the nodal voltages and [h(t)] is the vector of the current sources.

To obtain matrices [G] and [h(t)], the individual power system elements are represented by suitable discrete-time domain models. The continuous-time differential equations describing particular power system element are transformed into a discrete-time ones using the trapezoidal integration rule. To demonstrate the accuracy of that method, we will examine the model for a simple, ideal inductance.

After discretization of continuous-time differential equations for the simple inductance, it can be shown that the ratio between the continuos-time inductance (L) and equivalent discrete-time inductance (L_{eq}) is given by the equation [5]:

$$\frac{L_{eq}}{L} = \frac{\tan(\omega\Delta t/2)}{(\omega\Delta t/2)}$$

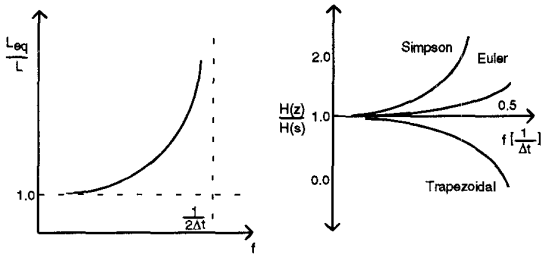

Fig. 3. L_{eq}/L Ratio

Fig. 4. Magnitude Distortion

From Fig. 3, this ratio clearly deteriorates as the frequency increases toward Nyquist frequency ($f_S/2$). The error introduced by the trapezoidal integration rule can be expressed more generally as the ratio of the continuous-time domain and discrete-time domain integrators H(s) and H(z). Fig. 4 shows the frequency dependence of the magnitude of this ratio for several integration rules. A similar analysis can be used to examine the phase error introduced by the different integrators. Table I shows some values of magnitude error for the trapezoidal rule for a simulation time step of 50μs.

Table I. MAGNITUDE ERROR DEPENDENCE ON FREQUENCY

f(Hz)	2000	4000	8000	10000
Error	3%	10%	60%	100%

Any realistic power system model will be a combination of simple and complex elements, with complex interactions between the errors introduced by each element. The propagation of the errors introduced by each element through the simulation is poorly understood at present, but since the overall simulation may be greater than, or less than, that of any single element, care should be taken to model each element as accurately as possible.

D. Network complexity

In analyzing the relation between the network complexity and time step, the first aspect that can be examined is the size of the network. Different tests have been performed using power system model shown in Fig. 5.

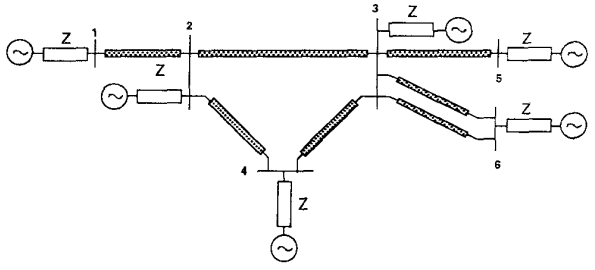

Fig. 5. Example system no. 1

The variable in these tests was the number of distributed transmission line models. First, all lines were represented using lumped parameter models. Then, the lumped parameter models were replaced by the distributed parameter models, one by one. The results of these tests reveal relations between the time step and the number and sizes of matrix diagonal blocks. The results are summarized in Table II.

Table II. TIME STEP VERSUS NETWORK SIZE

Test	#	Sizes of Blocks						Δt
Case	Lines	#1	#2	#3	#4	#5	#6	(μs)
1.	0	24	-	-	-	-	-	45.3
2.	1	24	-	-	-	-	-	47.1
3.	2	12	12	-	-	-	-	40.1
4.	3	9	3	12	-	-	-	38.3
5.	4	9	3	9	3	-	-	38.3
6.	5	6	9	3	3	3	-	38.3
7.	6	6	9	3	3	3	-	41.8
8.	7	6	6	3	3	3	3	40.1

An important characteristic of the *RTS's* solution method is that distributed parameter line model effectively decouples networks connected to the two terminals of the line. This characteristic can be employed to rearrange network matrix in block-diagonal form, giving a computationally more efficient solution procedure. Because of this, cases 1 and 2 (matrix form shown in Fig. 6a) required a larger time step than cases 3 to 6 (matrix form shown in Fig. 6b), where additional line sections were modelled with the distributed parameter line model. However, because the distributed line models are computationally more demanding than the lumped parameter line models, there is, eventually, an increase in the required time step, as indicated in case 7. This indicates that, as long as the introduction of these models results in a more sparse matrix, one should expect an improvement in the speed of computation. When the number of matrix diagonal blocks remains the same, the computational load of the more complex models will cause an increase in the required time step (compare case 1 versus case 2, and case 6 versus case 7).

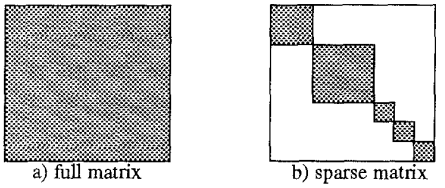

Fig. 6. Network matrix form

Additionally, it should be mentioned that distributed parameter line models can not be used if the wave travel time in any propagation mode is less than the simulation time step. Since the time step can not be set arbitrarily low in the real-time simulations, lumped parameter line models must usually be used for shorter lines.

Connected to the above point is the consideration of the presence of the frequency dependent (FD) parameter line models in the network. These models usually give better transient response in the zero propagation mode, but they are also far more computationally demanding than the constant parameter (CP) line models. As shown in Table III, the analysis done for the network shown in Fig. 7 reveals a drastic increase in the time step when FD line models are introduced. The user may try to keep FD line models in the network by using the models of the lower order. Experiments with the system of Fig. 8, comparing the use of 10 pole line models to the use of 24 pole line models, show a significant difference in the time step (see cases FD-10 and FD-24).

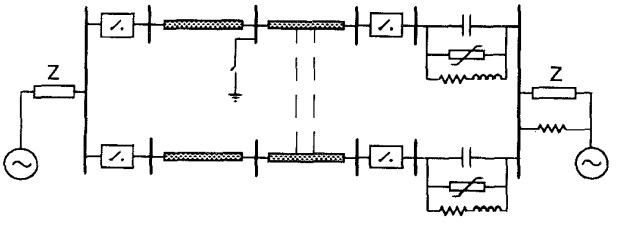

Fig. 7. Example System no. 2

Table III. TIME STEP: CP VERSUS FD LINE MODELS

Test Case	Single Lines	Double Lines	A(ω) Poles	CB Operat.	Δt (μs)
CP	2	1	-	7	49.4
FD-10	2	1	10	7	104.6
FD-24	2	1	24	7	193.3

Dynamic changes in either the system model, or in a model element, represent another aspect of the network complexity. Two types are especially important: circuit breaker operations (CB) and metal-oxide varistor operations (MOV). Both require a change of the block of the network matrix where the particular element is modeled. Although the *RTS* employs a rather efficient method of changing the network matrix [1], the number of arithmetic operations performed may still be significantly increased. A typical time step profile of the simulation, obtained measuring time necessary to compute one time step solution and transfer the result to the DSP subsystem, is shown in Fig. 8. It can be seen that CB operations cause a large increase in the time step of the iteration, while the increase due to MOV operations extends over the entire period of MOV activity.

The increase of the simulation time step caused by the CB operations is compensated, as it must be to maintain real-time operation, by the effective use of buffers. *RTS* uses a very efficient algorithm to represent both types of changes, it can exploit time delays associated with the operation of an actual circuit breaker to effectively run network simulation "ahead" of the change in network topology. Since these delays are typically 1-5 cycles (16-85 msec for a 60 Hz system) there is ample time to "make up the difference". This scheme enables the simulator to output its waveform samples with a time step of 64.7 μs for the case shown in Fig. 8.

After considering the design discussed above, the time step measurements summarized in Table IV are as expected: a typically large number of MOV operations results in an increase of the time step, while the much less frequent CB operations seemingly do not have any significant effect.

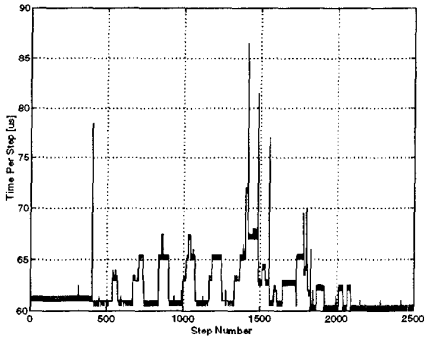

Fig. 8. Typical Time Step Simulation Profile

Table IV. TIME STEP: CB AND MOV OPERATIONS

Test Case	MOV Oper.	CB Oper.	Δt (μs)
1	-	1	48.5
2	-	7	49.4
3	1374	1	56.1

E. I/O Subsystem Characteristics

This section gives more details about the relation between the network simulation time step and real-time output time step, addressing two issues: instrument transformer and circuit breaker model implementation.

Instrument transformer and circuit breaker models are implemented in the DSP subsystem, which consists of four processors with an input clock of 40 MHz (instruction cycle T=60ns). Three processors are dedicated to servicing the individual I/O cabinets, providing, among other functions, instrument transformers modeling for each terminal. The forth processor performs service functions for the other three, including modeling the circuit breakers for each terminal.

The instrument transformer models are highly optimized, utilizing the full advantage of the processor architecture. By counting the number of the instructions, it is possible to calculate the time needed to compute one time step solution. It can be shown that computation time per each phase of a CT model is 40T and per each phase of a CCVT model 117T. That corresponds to 2.4 μs for CT and 7.0 μs for CCVT. The computation time for all three phases is three times the single phase computation time. The DSP models are effectively a constant time delay between the RISC output and the amplifier inputs, and since this delay is less than minimum simulation time step of the design (approximately 25 μs), there is no effect upon the transient waveform.

Circuit breaker models are implemented in the DSP subsystem separately from the rest of the network. Such a design enables one to attain stringent real-time requirements despite the high cost of circuit breaker operations. Utilizing inherent circuit breaker delays, the fact that the network simulation and circuit breaker models are decoupled, and the availability of enough memory on the DSP chips, real-time operation of the simulator can be optimized as discussed.

IV. SIMULATOR DESIGN UPGRADES

This section analyzes the relations between different aspects of the simulation time step and the computer platform of the simulator. As it is mentioned earlier, the hardware and software design of the simulator are centered around IBM's family of RISC computers. This design philosophy makes it possible to significantly increase the simulator's performance by simply replacing one computer with a more powerful one. Because it is a quite viable option, we will show here what it brings to a user.

The results of the analysis done for system no. 2 (Fig. 7) and system no. 3 (Fig. 9) are given in Table V.

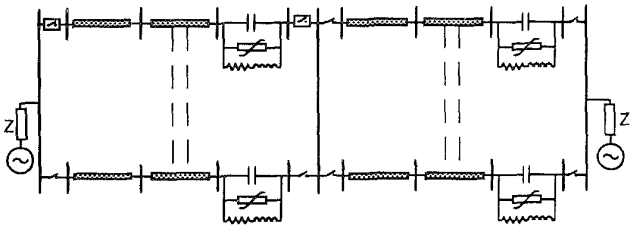

Fig. 9. Example System no. 3

Table V. TIME STEP ON DIFFERENT COMPUTERS

Model	SPEC int92	SPEC fp92	MFLOPs	System #2	System #3
250	62.6	72.2	19.5	162.4	329.2
580	73.3	134.6	38.1	85.3	182.4
590	117.0	242.4	130.4	55.1	97.1

There are several benefits in upgrading the real-time simulator to a faster computer platform. First, for the same power system model, a shorter simulation time step is possible, thus providing wider output signal bandwidth. At the same time, the accuracy of the signals is also increased because of its dependence upon the simulation time step (see Table I). Alternatively, more complex power system models can be used without increasing the time step. All the network complexity aspects that have been discussed earlier can be increased. For example, one can decide to increase the size of the network, while others may opt to include more complex element models in the network simulation. Regardless of the choice, greater accuracy is achieved by embracing more accurately the physical phenomena. The user has the capability of selecting the RISC machine, and thereby the simulator, which best fits the expected demands.

V. CONCLUSIONS

The discussion given in this paper leads to the following conclusions:

- The simulation time step is a critical design and application parameter that needs to be closely defined and understood
- The simulation time step relates to a number of design and application issues such as: frequency bandwidth, simulation accuracy, network complexity, and I/O subsystem requirements
- Given the tradeoffs between the various application aspects, a simulator design should allow the user the greatest possible amount of flexibility in selecting the time step in order to insure that the widest application of the simulator is possible
- A simulator design that allows for a direct upgrade of the simulator computer to a higher performance model provides for a direct increase in the time step flexibility whenever the user needs such an increase

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